HITACHI

No. 0800

HDR080

SERVICE MANUAL
MANUEL D'ENTRETIEN
WARTUNGSHANDBUCH

CAUTION:
Before servicing this chassis, it is important that the service technician read the “Safety Precautions” and “Product Safety Notices” in this service manual.

ATTENTION:
Avant d’effectuer l’entretien du châssis, le technicien doit lire les «Précautions de sécurité» et les «Notices de sécurité du produit» présentés dans le présent manuel.

VORSICHT:
Vor Öffnen des Gehäuses hat der Service-Ingenieur die „Sicherheitshinweise“ und „Hinweise zur Produktsicherheit“ in diesem Wartungshandbuch zu lesen.

Data contained within this Service manual is subject to alteration for improvement.

Les données fournies dans le présent manuel d’entretien peuvent faire l’objet de modifications en vue de perfectionner le produit.

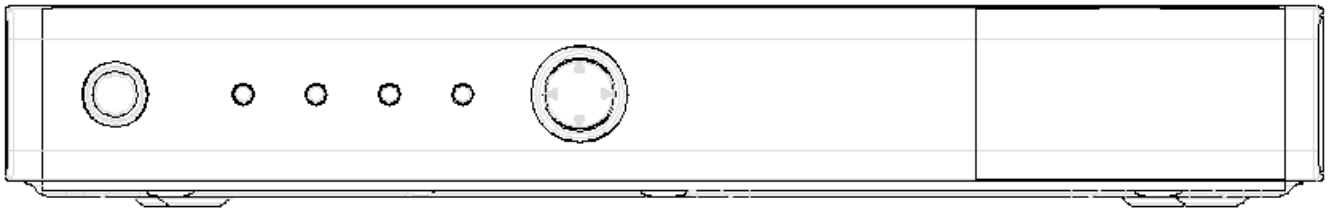
Die in diesem Wartungshandbuch enthaltenen Spezifikationen können sich zwecks Verbesserungen ändern.

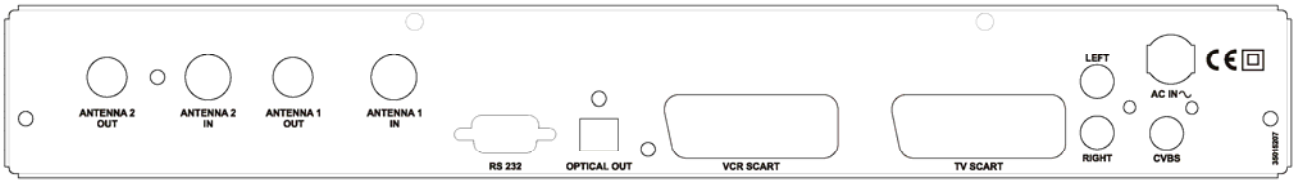
SPECIFICATIONS AND PARTS ARE SUBJECT TO CHANGE FOR IMPROVEMENT

Digital Set Top Box

October 2007

TERRESTRIAL STB MODELS





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GENERAL DESCRIPTION

Major functional blocks are discussed briefly in this section. A more detailed description is contained later in the document.

16mb31-1 Mainboard

STI5100 (IC101)

1. Introduction

The STi5100 is a low-cost Omega2 (The STBus multipath unified interconnect provides high on-chip bandwidth and low latency accesses between modules. The interconnect operates hierarchically, with latency-critical modules placed at the top level. The multipath router allows simultaneous access paths between modules, and simultaneous read and write phases from different transactions to and from the modules. Split transactions maximize the use of the available bandwidth.) MPEG device that delivers high performance and integrates features that provide an overall system cost reduction. The device implements a fully unified DDR SDRAM based memory architecture and integrates the Omega2 video decoder cell together with a blitter engine and a multichannel DMA controller to provide enhanced performance for graphics and real-time stream transfers.

DVR applications are supported by a dual-stream deMUX and using an HDD connected either to the FMI or USB 2.0 port.The STi5100 includes transport stream routing and strobe decoding logic for DVB-CI and CableCard (formerly known as POD) modules to reduce implementation cost.

2. Technical Specification

- **Features**
- **Enhanced ST20 32-bit VL-RISC CPU**
  - 243 MHz, 8Kbyte ICache, 8Kbyte DCache, 4Kbyte SRAM
- **Unified Memory Interface**
- **Dual Transport Stream Merger**
  - Supports DVB and DIRECTV .
  - Integrated DES-ECB, DVB and ICAMdescramblers
  - NDS RASP compliant
  - Low cost DVB-CI and Cable Card support
- **MPEG-2 MP@ML Video Decoder**
  - Trick modes including smooth fast forward andrewind
- **Audio**
  - MPEG-1 layers I/II, MP3
  - Dolby . Digital decoding

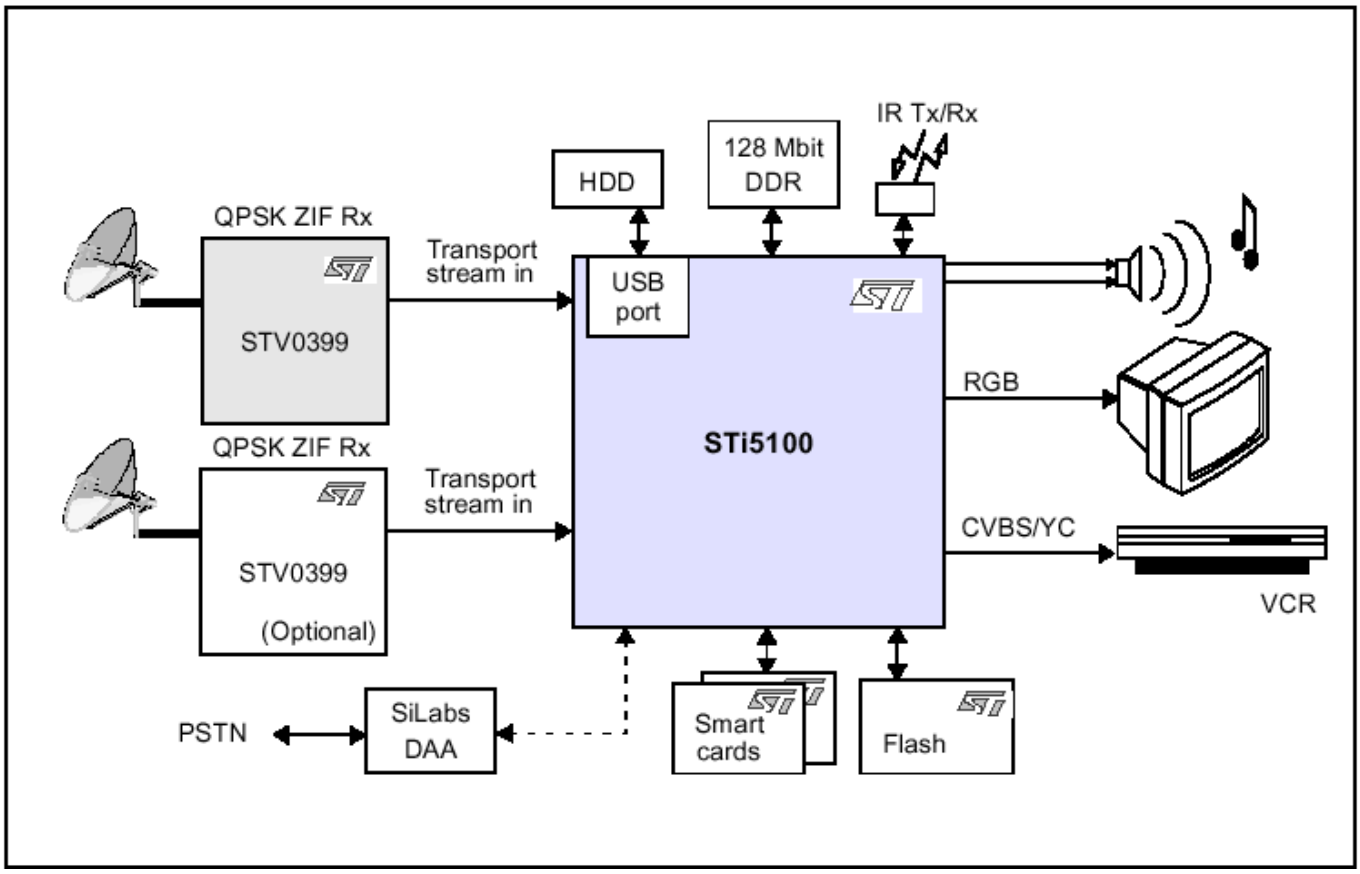
  - Dolby Pro Logic . compatible output
  - PCM input, mixing and sample rate conversion
  - SRS/TruSurrondXT . virtual surround sound
  - Simultaneous MPEG audio decode and outputof Dolby streams
- **Graphics/Display**
  - 4 display planes
  - 2, 4 and 8 bpp CLUT graphics, 256 x 30 bits(AYCBCr) CLUT entries
  - 16 bpp true color graphics
  - Alpha blending, antialiasing, antiflutter,antiflicker filters

- **PAL/NTSC/SECAM encoder**
  - RGB, CVBS, Y/C and YUV outputs with 10-bitDACs
  - CGMS, Teletext, WSS, VPS and close caption
- **On-Chip Peripherals**
  - 4 ASCs (UARTS)
  - 4 parallel 8-bit I/O banks
  - 2 smartcard interfaces and clock generators
  - 3 SSCs for I²C/SPI master/slave interfaces
  - Silicon Labs line side (DAA) interface
  - High-speed USB OHCI/EHCI compliant host interface
  - DiSEqC interface

3. Architecture overview

The figure below shows the architecture of the Sti5100.

This chapter gives a brief overview of each of the functional blocks of the STi5100.



4. STi5100 functional modules

4.1 Memory subsystem

The STi5100 has a local memory interface (LMI) and a flash and peripheral interface (FMI). The STi5100's local memory interface is used for all data requirements in unified memory applications, including graphics, video and audio buffers. It provides 16-bit wide DDR SDRAM support only at up to 166 MHz. The FMI provides support for 16-bit wide peripherals, flash and synchronous flash.

Local memory interface (LMI)

The LMI is a 16-bit wide DDR SDRAM interface with a peak bandwidth of 664 Mbyte/s (166 MHz). It supports one bank of 128-Mbit, 256-Mbit, or 512-Mbit DDR SDRAM. The LMI provides a fully cacheable address space for data and instructions, with data cacheability controlled in 512 Kbyte blocks for up to 8 Mbytes.

Flash and peripheral memory interface (FMI)

The FMI provides a glueless interface to SRAM, flash, SFlash and peripherals, in up to four configurable banks over a 16-bit wide interface. Bus cycle strobe timings can be programmed from 0 to 15 phases for slower peripherals. The FMI output drive of the STi5100/STi5101 is programmable on a bus-by-bus basis. Support is provided for connection to an ATAPI HDD.

4.2 Transport stream processing

The STi5100 supports dual independent transport stream inputs using an SRAM-based packet merger and a single programmable transport interface (PTI). The merger buffers a packet pair per channel. The incoming transport packets are tagged with a source ID and a time stamp.

Programmable transport interface (PTI)

The PTI performs transport-stream descrambling, demultiplexing and data filtering. PESdata is transferred by DMA to audio and video decoders using circular buffers. Section data is transferred by DMA to separate buffers for further processing by the CPU.

- DIRECTV and DVB transport streams can be handled by the PTI with data rates up to 138 Mbit/s.
- The PTI performs PID filtering to select audio, video and data packets to be processed. 96 PID slots can be supported by the PTI.
- The PTI can descramble streams using the following ciphers:
  - DES-ECB,
  - DES-CBC including DVS-042 and cipher text stealing termination block handling,
  - DVB-CSA,
  - NDS specific streams can also be supported for integrated ICAM functionality.
- The PTI has a section filter core that filters DVB and DIRECTV standard sections. Four filtering modes are available:
  - wide match mode: 48x 16-byte filters,
  - long match mode: 96x 8-byte filters,
  - positive/negative mode: 48x 8-byte filters with positive/negative filtering at the bit level.

Matching sections are transferred to memory buffers for processing by software.
When the PTI is required to output a transport stream, it can output the entire transport stream or selected packets filtered by PID. A latency counter is provided to ensure packet timing is preserved. Packet substitution can also be performed.

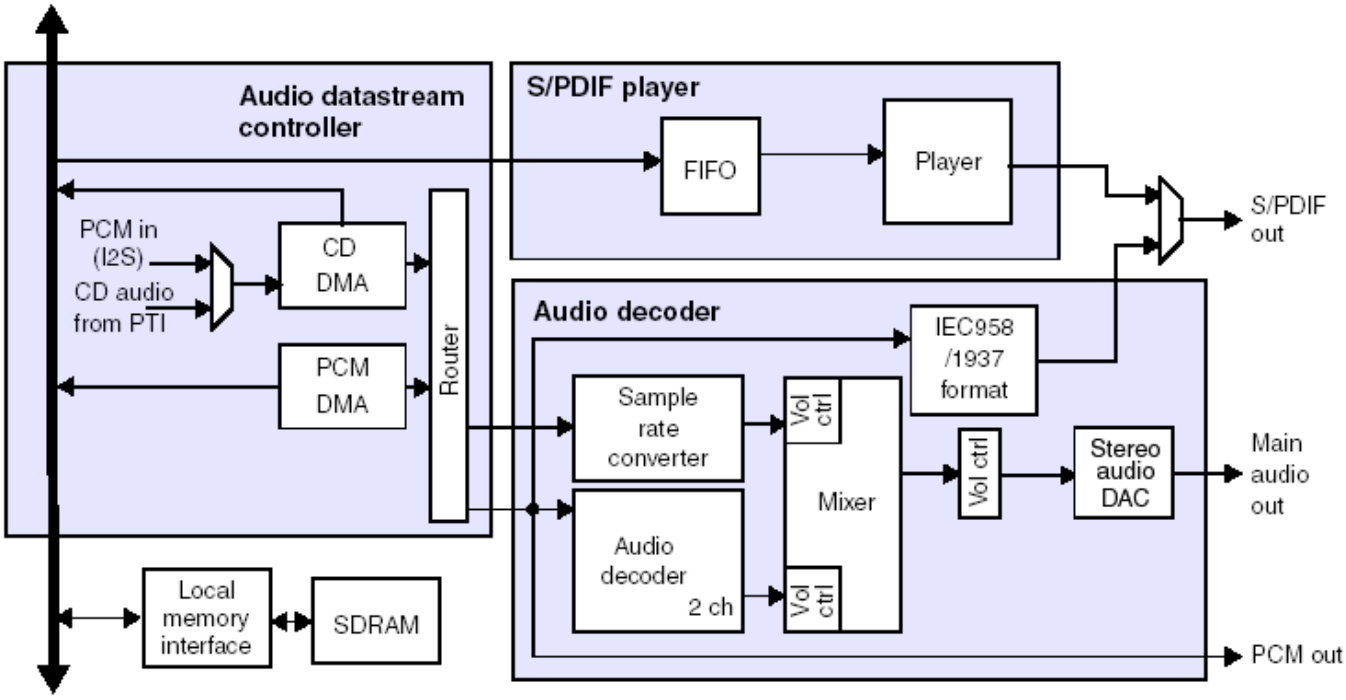
4.3 Audio subsystem

The audio subsystem supports multichannel audio decoding and mixing with internal PCM files. Decoding of MPEG-1 layers I, II, MP3 and Dolby Digital stereo are supported.Decoded multichannel audio is downmixed before emerging as stereo or Dolby Pro Logic compatible encoded audio. Simultaneous MPEG audio decoding and output of Dolby streams on the S/PDIF is also supported. SRS Labs' TruSurroundXT is also provided for two speaker virtual surround sound. The integrated DACs provide analog stereo output directly from the device using a single-ended interface.Multichannel streams can be passed through to the IEC958 output for external decoding. Audio sample rates of 32 kHz, 44.1 kHz and 48 kHz are supported.The audio digital-to-analog converter is a high performance stereo audio converter operating at 256 Fs system clock using single-ended voltage. This DAC accepts a 24-bit input data in I 2 S format from the audio decoder macro block and converts them into up to 2 Vrms output voltage. Digitized analog audio can also be input to the STi5100 using the PCM input interface and buffered in memory via DMA. 26/830 STMicroelectronics Confidential 7603604B The audio subsystem consists of the following units.

- **Audio datastream controller**

The audio datastream controller receives, buffers and reformats audio data. It handles up to three audio data flows concurrently.
It receives a raw PCM stream from an external source via the PCM input interface or receives a compressed data stream from an internal source such as the PTI and stores this in a memory buffer via DMA. This is used to buffer and play the main audio for the digital or analog program.

It receives a PCM file or stream from a memory buffer via DMA and delivers this to the audio decoder's second input for sample rate conversion and mixing with the main audio.
The router is able route either source to either input of the audio decoder.



- **Audio decoder 24-bit audio digital signal processor**

The digital signal processor processes audio streams sent to it by the CD player and PCM file player.

- **S/PDIF player**

The independent S/PDIF player can output a compressed Dolby Digital audio stream independently of the stream being decoded.

- **IEC958/IEC1937 formatted output**

The audio decoder outputs IEC958/IEC1937 formatted CD or PCM audio received from the audio decoder.

- **1-channel PCM output interface**

The PCM output interface outputs PCM audio received from the audio decoder.

- **Integrated 24-bit stereo audio DAC system**
- **Programmable tone generation for dish alignment**

4.4 Internal peripherals

The STi5100 has many dedicated internal peripherals for digital TV receiver applications, including:

- 2 smartcard controllers,
- 4 ASCs (UARTs), two of which are generally used by the smartcard controllers, teletext serializer and DMA,
- 3 SSCs for I 2 C master/slave interfaces, with SPI support,
- 4.5 GPIO ports, with a further 1.5 ports mapped to transport pins,
- 1 PWM module,
- a multichannel, infrared blaster/decoder interface module,

- a modem analog front-end interface (MAFE),
- DVB common interface support,
- CableCard support,
- fully integrated digital clock recovery for MPEG (replacement for VCXO),
- USB 2.0 host, OHCI/EHCI compliant,
- interface to SiLabs line side device (DAA),
- an interrupt level controller,
- a low-power/RTC/watchdog controller,
- DCU toolset support,
- a JTAG/TAP interface.

4.5 Clock generation

All system clocks are generated using the clock generator block. This contains two high-frequency PLLs (600 MHz) that are divided down to produce a series of phase-related programmable clock channels. The guaranteed phase relationship between these channels simplifies interconnect bridging between different subsystem modules and gives lower latency compared to a fully asynchronous clocking scheme.
The STi5100 is a clock master. The flash clock output may be phase aligned to optimize the external bus performance of the FMI.
Digital clock recovery for MPEG (DCO) has been integrated using a special purpose frequency synthesizer, thus removing the need for an external varactor diode or VCXO module. An external VCXO can still be used for genlocking applications.

Symbol	Parameter	Min	Typical	Max	Units	Notes
VI	Input voltage (3.3 V I/O only)	0		3.6	V	1
VI35	Input voltage (3.3 V / 5 V tolerant I/O)	0		5.5	V	2
C_L	Load capacitance per pin			100	pF	
TA	Operating temperature (ambient)	0		70	°C	

Symbol	Parameter	Min	Typical	Max	Units	Notes
VDD	Positive core supply voltage	1.08	1.2	1.32	V	
VDD25	Positive I/O supply voltage	2.3	2.5	2.7	V	
VDD33	Positive I/O supply voltage	3.0	3.3	3.6	V	
V_{IH}	Input logic 1 voltage (3.3 V I/O only)	2.0			V	
V_{IH5}	Input logic 1 voltage (5 V tolerant I/O only)	2.0		5.5	V	
V_{IL}	Input logic 0 voltage			0.8	V	
I_{IN}	Input current (input pin)			5	µA	1
I_{OZ}	Off state digital output current			50	µA	
IWP_U	Input weak pull-up current			110	µA	
IWP_D	Input weak pull-down current			110	µA	
V_{OH}	Output logic 1 voltage	VDD33 - 0.15			V	2
V_{OL}	Output logic 0 voltage			0.15	V	3
C_{IN}	Input capacitance (input pins)			10	pF	
C_{IO}	Input capacitance (bidirectional pins)			15	pF	
C_{OUT}	Output capacitance			15	pF	
V_{HYS}	Hysteresis voltage (3 V/5 V tolerant I/O)	0.495		0.620	V	4

DDRAM 4M x 16Bit x 4 Banks Double Data Rate SDRAM (IC2) K4H561638F

FEATURES

VDD : 2.5V± 0.2V, VDDQ : 2.5V± 0.2V for DDR266, 333

- VDD : 2.6V± 0.1V, VDDQ : 2.6V± 0.1V for DDR400
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe [DQS] (x4, x8) & [L(U)DQS] (x16)
- Four banks operation
- Differential clock inputs(CK and /CK)
- DLL aligns DQ and DQS transition with CK transition
- MRS cycle with address key programs
  - Read latency : DDR266(2, 2.5 Clock), DDR333(2.5 Clock), DDR400(3 Clock)
  - Burst length (2, 4, 8)
  - Burst type (sequential & interleave)
- All inputs except data & DM are sampled at the positive going edge of the system clock(CK)
- Data I/O transactions on both edges of data strobe

- Edge aligned data output, center aligned data input
- LDM, UDM for write masking only (x16)
- DM for write masking only (x4, x8)
- Auto & Self refresh
- 7.8us refresh interval(8K/64ms refresh)
- Maximum burst refresh cycle : 8
- 66pin TSOP II Leaded & Pb-Free(RoHS compliant) package

GENERAL DESCRIPTION

The K4H561638F is 268,435,456 bits of double data rate synchronous DRAM organized as 4 x 4,194,304 words by 16bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous features with Data Strobe allow extremely high performance up to 400Mb/s per pin. I/O transactions are possible on both edges of DQS.Range of operating frequencies, programmable burst length and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

HY29LV320 32 Mbit (2M x 16) Low Voltage Flash Memory (IC1)

Low Voltage Single Supply Flash Memory

Single Power Supply Operation

– Read, program and erase operations from 2.7 to 3.6 volts

– Ideal for battery-powered applications

_ High Performance

– 70, 80, 90 and 120 ns access time versions for full voltage range operation

_ Ultra-low Power Consumption (Typical/ Maximum Values)

– Automatic sleep/standby current: 0.5/5.0 µA

– Read current: 9/16 mA (@ 5 MHz)

– Program/erase current: 20/30 mA

_ Top and Bottom Boot Block Versions

– Provide one 8 KW, two 4 KW, one 16 KW and sixty-three 32 KW sectors

_ Secured Sector

– An extra 128-word, factory-lockable sector available for an Electronic Serial Number and/or additional secured data

_ Sector Protection

– Allows locking of a sector or sectors to prevent program or erase operations within that sector

– Temporary Sector Unprotect allows changes in locked sectors

_ Fast Program and Erase Times (typicals)

– Sector erase time: 0.5 sec per sector

– Chip erase time: 32 sec

– Word program time: 11 µs

– Accelerated program time per word: 7 µs

_ Automatic Erase Algorithm Preprograms and Erases Any Combination of Sectors or the Entire Chip

_ Automatic Program Algorithm Writes and Verifies Data at Specified Addresses

_ Compliant With Common Flash Memory Interface (CFI) Specification

– Flash device parameters stored directly on the device

– Allows software driver to identify and use a variety of current and future Flash products
_ **Minimum 100,000 Write Cycles per Sector**
_ **Compatible With JEDEC standards**
– Pinout and software compatible with single-power supply Flash devices
– Superior inadvertent write protection
_ **Data# Polling and Toggle Bits**
– Provide software confirmation of completion of program and erase operations
_ **Ready/Busy (RY/BY#) Pin**
– Provides hardware confirmation of completion of program and erase operations
_ **Write Protect Function (WP#/ACC pin)**
- Allows hardware protection of the first or last 32 KW of the array, regardless of sector protect status
_ **Acceleration Function (WP#/ACC pin)**
- Provides accelerated program times
_ **Erase Suspend/Erase Resume**
– Suspends an erase operation to allow reading data from, or programming data to, a sector that is not being erased
– Erase Resume can then be invoked to complete suspended erasure
_ **Hardware Reset Pin (RESET#) Resets the Device to Reading Array Data**
_ **Space Efficient Packaging**
– 48-pin TSOP and 63-ball FBGA packages

16tut36-2 tuner board

STV0360/0361(COFDM demodulators IC for terrestrial TV set-top box)

STMicroelectronics complements the world leading range of MPEG-2 decoders with a range of COFDM demodulators for digital terrestrial applications. The STV0360 and STV0361 demodulators are high performance COFDM (Coded Orthogonal Frequency Division Multiplex) demodulators with built in A/D converters. They perform all the demodulation functions to extract the MPEG-2 transport stream from the tuner input.

- DVB-T (ETS 300 744), NORDIG II and NORDIG Unified 1.0.1 compliant1
- Inputs for direct IF, eliminating the need for a down-converter in the tuner
- Adaptative channel correction in both time and frequency, providing excellent performance, event in the presence of noise or significant Doppler shift.
- Dual Automatic Gain Controller (AGC) to seamlessly interface with all tuners characteristics
- Support for 2K/8K carrier detection modes
- PGA (Programmable Gain Amplifier) increasing flexibility to enhance tuner power matching
- Additional A/D converter to directly monitor the input level of the new generation of tuners

Figure 1: Parallel connection of STi5100 nd STV0360

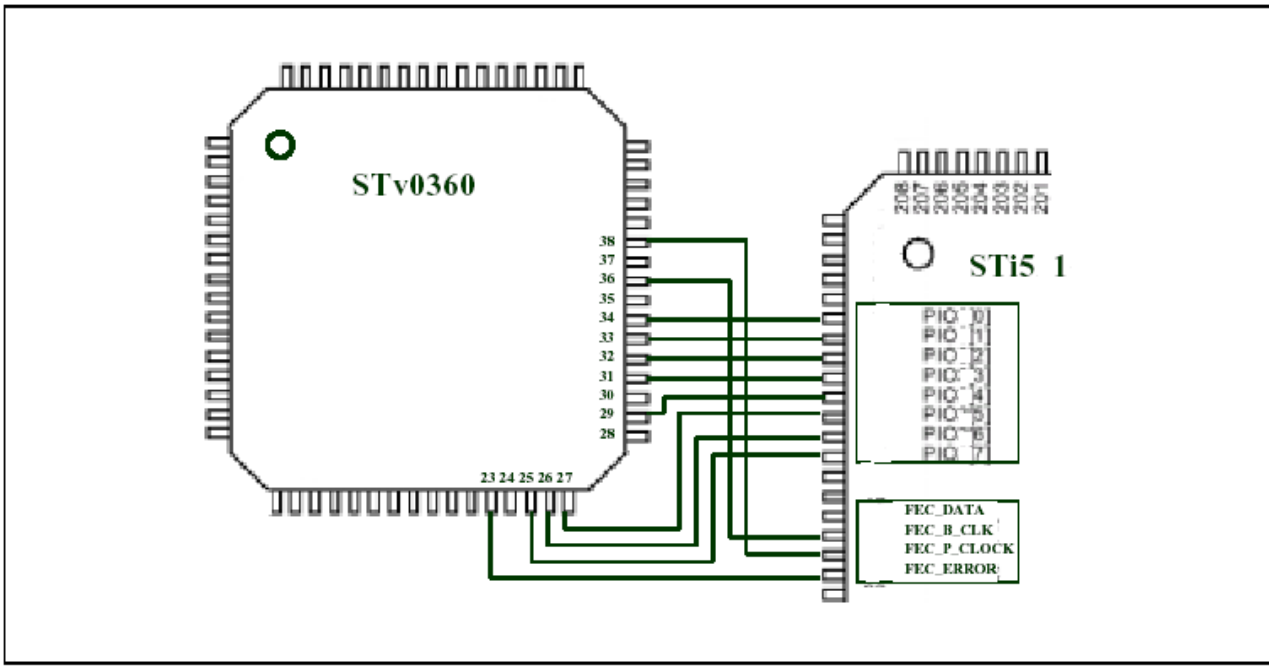
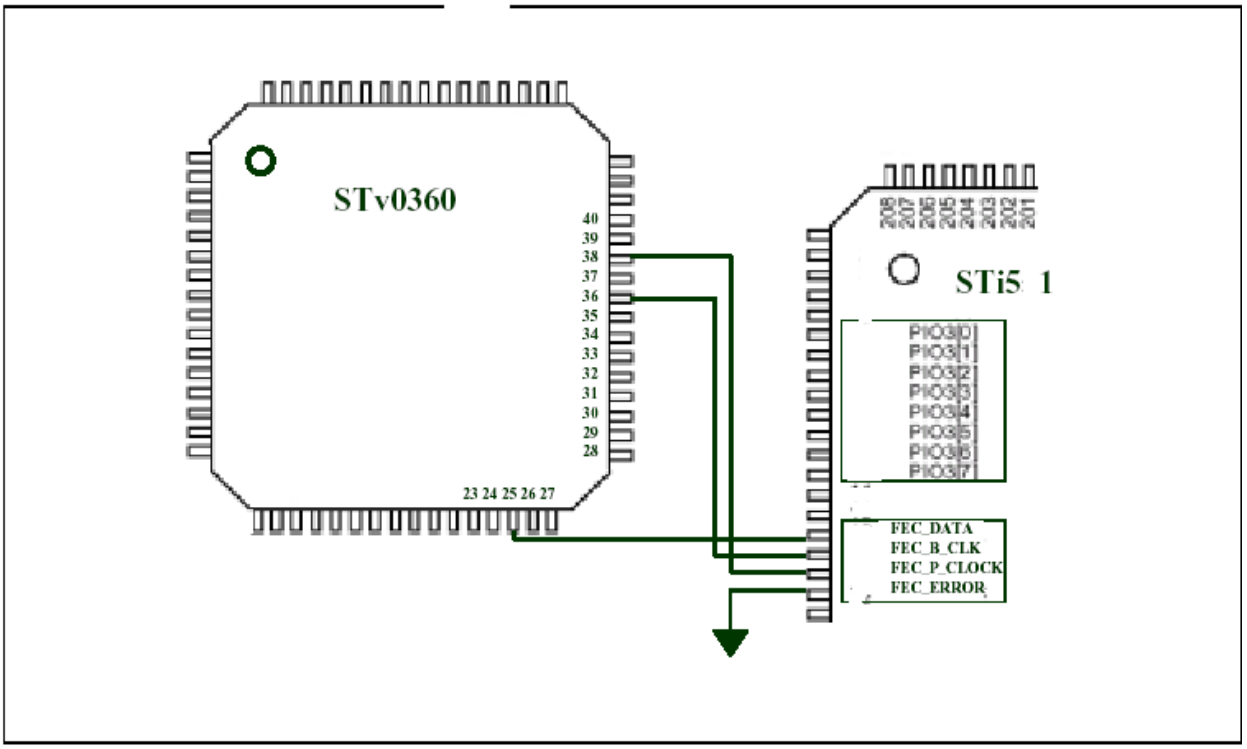


Figure 4: Serial connection of STi5100 and STV0360



TUNER (DTOS449IV241B-DTOS443PV241B)

DESCRIPTION

Receiving System : Designed to cover the air channels in UHF including digital terrestrial channels for CCIR system.

Receiving Channel : 47MHz ~ 862MHz

Intermediate Frequency : Digital(center) 36.125 MHz

Input Impedance : 75Ω, Unbalanced.

IF Output Impedance : 10Ω, Balanced.

Band Change-Over System : PLL system.

Tuning System : PLL system.

Built in DC/DC convert driver get rid of a 33V supply voltage.

Internal RF AGC function :

Built in wideband AGC detector with 6 programmable take-over points

Narrow band output to be filtering by a 7/8MHz switchable SAW filter.

Built in the additional IF amplifier with AGC circuit.

PIN	CONNECTION
1	BA (ANT's booster)
2	N.C
3	AS
4	SCL
5	SDA
6	B+(5V, Loopthrough)
7	BP(5V)
8	AGC2 (IF AGC)
9	VT for monitoring
10	IFOUT2
11	IFOUT1
12	RF INPUT
13	RF OUTPUT

ELECTRICAL CHARACTERISTICS

Input Frequency Range

VHF-low Band	: 47 MHz ~ 174MHz
VHF-High Band	: 174MHz ~ 470MHz
UHF Band	: 470MHz ~ 862MHz
RF Input Return loss	: -8dB typ. -6dB max.
Voltage Gain	: 73dB min. 77dB typ.
Loopthrough Gain(for 47 to 862MHz)	: 1 ± 3 dB
Input Signal level	: -85dBm min. (-12dBm symmetrical output)

Noise Figure

Tuner IF output	: 5dB typ. 8dB max. (at max. gain)
Loop through	: 6dB typ. 8dB max.

Gain deviation	: 4dB typ. 7dB max.

IF Response curve

Amplitude ripple in band (AGC Volt 4.0 ~ 0.8V) : ± 3dB max.

1) Center± 4MHz (Above 306MHz)

2) Center± 3.5MHz (Below 300MHz)

3dB bandwidth in band (AGC Volt 4.0 ~ 0.8V)

: 7/8MHz (switchable SAW Filter)

AGC Range

RF AGC (Vagc = 4 ~ 0.5V)	: 40dB min. 45dB typ.
IF AGC (Vagc = 2 ~ 0.5V)	: 46dB min. 53dB typ.

IF Rejection(Measured @36.125MHz)

: 60dB min. 75dB typ.

Image Rejection	: 50dB min. 55dB typ.
Osc stop voltage	: 4.5V max.

Ant leakage

500 to 1000 MHz	: 40dBμV max
1000 to 1750 MHz	: 50dBμV max
IF leakage	: 80dBμV max.
Step Frequency	: 166.67kHz (refer 5-4)
Reference X-tal Frequency	: 4MHz

Phase Noise

@ 1kHz	: -85dBc/Hz typ. -78dBc/Hz max.
@ 10kHz	: -85dBc/Hz typ. -78dBc/Hz max.
@100kHz	: -105dBc/Hz typ. -100dBc/Hz max.

16sc31-2 scart board

STV6413Audıo/Vıdeo Switch Matrix(IC200)

- **I²C Bus Control**
- **Standby Mode with Interrupt Signal Output**
- **Video Section**
- 3 CVBS Inputs, 2 CVBS Outputs
- 3 Y/C Inputs, 2 Y/C Outputs
- 6 dB Gain on all CVBS/Y and C Outputs
- Integrated 150 W Buffers
- 2 RGB/FB Inputs, 1 Tri-state RGB/FB Output with 6 dB Adjustable Gain (from +3 dB to +9 dB)
- Video Muting on all Outputs
- 2 Slow Blanking Inputs/Outputs
- Sync Bottom Clamp on all CVBS/Y and RGB
- Inputs, Average Clamp on C Inputs
- Bandwidth: 15 MHz
- Crosstalk: 50 dB Minimum
- **Audio Section**
- 3 Stereo Inputs, 3 Stereo Outputs
- Stereo-to-Mono Sound Capability
- 0/6/9 dB Selectable Gain on one Stereo Input
- Full Range Volume Control with Soft Control
- Audio Muting on all Outputs

Supply Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Digital Supply Voltage		4.75	5	5.25	V
V_{CCAO}	Audio Operating Supply Voltage	- Decoupling capacitor on V_{CCA} - Connected to V_{CCA}	11.2 8.5	12 9	12.8 9.5	V
V_{CC}	Video Operating Supply Voltage		4.75	5	5.25	V
V_{CC12}	Slow Blanking Control Supply Voltage		11.2	12	12.8	V

Thermal Data :

Symbol	Parameter	Value	Unit
R_{thJC}	Junction-to-Case Thermal Resistance		°C/W
R_{thJA}	Junction-to-Ambient Thermal Resistance[1]	48	°C/W
T_J	Maximum Recommended Junction Temperature		°C

16PW36-2 Power board

16MB07 E3 Board Power Consumption			
STAND_BY	Voltage	Current mA	Power Watts
			11.7W
	+12V		
	+5V		
	+3V3		----
POWER_ON	Voltage	Current mA	Power Watts
			19W
	+12V		
	+5V		
	+3V3		

The TOPSwitch concept is used for power supply. TOP 234Y (IC1) is designed to work until 50 Watts in family of TOPSwitch_FX with 5 pins. The receiver works between 85 and 265 VAC mains voltage by using TOP 234Y in SMPS (Switch Mode Power Supply).
In SMPS applications, secondary voltage regulation is adjusted according to the feedback voltage from the secondary side of transformer. The feedback voltages are 3.3V and 5V. This is connected to the comparator pin of TOP 234Y (IC1-pin1) via IC2 (Optocoupler). The comparator pin also protects the box against short circuits and overload. The supply voltage of TOP233Y(IC1) is between 2V and 3V at pin2. The TOP 234Y works at a fixed frequency. This frequency is fixed by RC oscillator at pin1. Pin3 and pin4 are ground and pin5 is the drain of the MOSFET, which is inside the TOP 234Y. Due to changes in Vcc, TOP234Y adjusts the duty cycle of the square wave in drain pin and regulates the secondary side of the transformer. Vcc voltage which changes between 2V and 3V is also used to regulate and protect.

Output voltages of the transformer (TR2):

(i) 3.3V: 5100 IC (IC101),flash memory (IC 1), tuner and other components.
(ii) 5V: Front panel board, Tuner , and some ICs and circuits.
(iii) 12V: hard disk and some other ic and circuits
(iv) -25V :flaman voltage

16fp38-3 front board

VFD Driver/Controller IC PT6311(IC2)

• CMOS Technology
• Low Power Consumption
• Key Scanning (12 x 4 matrix)
• Multiple Display Modes: (12 segments, 16 digits to 20 segments, 8 digits)
• 8-Step Dimming Circuitry
• LED Ports Provide (5 channels, 20 mA max.)
• 4- Bits General Purpose Input Ports Provided
• Serial Interface for Clock, Data Input, Data Output, Strobe Pins
• No External Resistors Needed for Driver Outputs

Parameter	Symbol	Ratings			Unit
		Min.	Typ.	Max.	
Logic Supply Voltage	VDD	4.5	5	5.5	V
High-Level Input Voltage	VIH	0.7VDD	-	VDD	V
Low-Level Input Voltage	VIL	0	-	0.3VDD	V
Driver Supply Voltage	VEE	VDD -35	-	0	V

Front board connector – PL5	
Pin	Description
1	+12VSTB
2	GND
3	GND
4	+5VSTB

Front board Connector – PL811	
Pin	Description
1	+5V
2	GND
3	SENSE
4	IR_IN
5	DISP DATA
6	DISP CLK

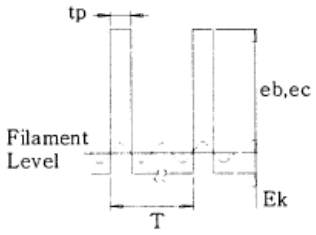
Pin Name	I/O	Description	Pin No.
SW1 to SW4	I	General Purpose Input Pins	1 to 4
DOUT	O	Data Output Pin (N-Channel, Open-Drain) This pin outputs serial data at the falling edge of the shift clock (starting from the lower bit).	5
DIN	I	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit).	6
NC	-	No Connection	7
CLK	I	Clock Input Pin This pin reads serial data at the rising edge and outputs data at the falling edge.	8
STB	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this in is "HIGH", CLK is ignored.	9
K1 to K4	I	Key Data Input Pins The data inputted to these pins is latched at the end of the display cycle.	10 to 13
VDD	-	Logic Power Supply	14, 33, 45
SG1/KS1 to SG12/KS12	O	High-Voltage Segment Output Pins Also acts as the Key Source.	15 to 26
SG20/GR9 to SG19/GR10 SG18/GR11 to SG13/GR16	O	High-Voltage Segment/Grid Output Pins	36 to 35 32 to 27
VEE	-	Pull-Down Level	34
GR1 to GR8	O	High-Voltage Grid Output Pins	44 to 37
LED1 to LED5	O	LED Output Pin	50 to 46
GND	-	Ground Pin	51
OSC	I	Oscillator Input Pin A resistor is connected to this pin to determine the oscillation frequency.	52

VACUUM FLUORESCENT DISPLAY

RECOMMENDED OPERATING CONDITION #5)

Item	Symbol	Min.	Typ.	Max.	Unit
Filament Voltage #2)	Ef	3.78	4.20	4.62	Vac
Peak Anode Voltage	eb	25.0	28.0	31.0	Vp-p
Peak Grid Voltage	ec	25.0	28.0	31.0	Vp-p
Cut-Off Bias Voltage	Ek	6.0	—	9.0	Vdc
Duty Factor	Du	—	1/14	—	—
Pulse Width	tp	—	100	—	μs
Operating Temperature	Topr	-20	—	+70	℃
Storage Temperature	Tstg	-55	—	+85	℃

ELECTRICAL CHARACTERISTICS

Item	Test Condition	Symbol		Min.	Typ.	Max.	Unit
Filament Current	Ef= 4.2 Vac ,eb=ec=0	If		135	150	165	mAac
Anode Current #1)	Ef= 4.2 Vac eb= 28.0 Vp-p ec= 28.0 Vp-p	ib	4G ~ 13G	—	4.0	8.0	mAp-p
			1G, 3G	—	15.0	30.0	
			2G	—	16.0	32.0	
Grid Current #1)	Duty= 1/14 tp= 100 μs tb= 0 μs	ic	4G ~ 13G	—	5.0	10.0	mAp-p
			1G, 2G	—	15.0	30.0	
			3G	—	13.0	26.0	
Brightness		GREEN		102	204	—	ft-L
		Rsh.O.		10	20	—	
Brightness Ratio Between Digits	(All Segs are lit)	L(Max.) / L(Min.)		—	—	2	
Grid Cut-Off Voltage #3)	Ef= 4.2 Vac, Eb= 28.0 Vdc, Ec=Vary	Ecco		(-6.0)	—	—	Vdc
Anode Cut-Off Voltage #3)	Ef= 4.2 Vac, Du= 1/14 ec= 28.0 Vp-p, Eb= Vary	Ebco		(-6.0)	—	—	Vdc

USED IC LISTS

MAINBOARD (16MB31-1)

Sti5100 (IC101)	Set Top Box Backend Decoder with Integrated Host Processor
MAX232 (IC601)	RS232 Driver / Receiver
74LVC244 (IC878)	IC 3-ST BUFFER
74LVX00 (IC902)	Low Voltage Quad 2-Input NAND Gate
74LVT14 (IC903)	3.3V Hex inverter Schmitt trigger
74LVTH244A (IC900)	Low Voltage Octal Buffer/Line Driver
FLASH (IC1)	32MBIT 3.3V ROHS
74LVTH16245A (IC901)	Low Voltage 16-Bit Transceiver with 3-STATE Outputs
LM1117 (IC500 ,IC473)	LDO 1.8V/800mA
LDO (DPAK) (IC606)	1.2V/800mA
REG LM7808 8V/1A (IC102)	1A REGULATORS
K4H561638F (IC2)	IC DDRRAM16MX16

POWER BOARD (16PW36-2)

TOP233Y (IC1)	SMPS primary IC
SFH617A (IC2)	Optocoupler
TL431(IC3)	Programmable Precision Reference
LM7812 (IC5)	12V Voltage Regulator

SCART BOARD (16SC31-2)

STV6414 (IC200)	IC SWITCH A/V

FRONT BOARD (16FP38-3)

IC PT6311(IC2)	VFD Driver/Controller

CONNECTORS

Power Connector – PL451	
Pin	Description
1	+12V
2	GND
3	GND
4	5V
5	+3V3
6	+3V3
7	STBY
8	NC
9	NC

Front Panel Connector – PL609	
Pin	Description
1	+5V
2	GND
3	SENSE
4	IR_IN
5	DISP DATA
6	DISP CLK

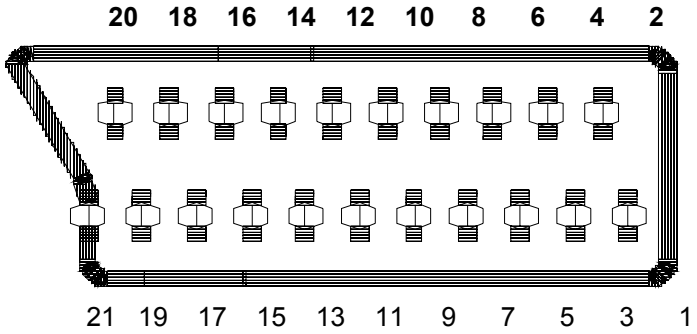
Hard disk power – PL404	
Pin	Description
1	+12VSTB
2	GND
3	GND
4	+5VSTB

Fan power – PL450	
Pin	Description
1	NC
2	+5V
3	GND

Hard disk data Connector – PL900			
Pin	Description	Pin	Description
1	HDDRESET	21	GND
2	GND	22	GND
3	HBUFDATA7	23	H_DIOW
4	HBUFDATA8	24	GND
5	HBUFDATA6	25	H_DIOR
6	HBUFDATA9	26	GND
7	HBUFDATA5	27	IORDY
8	HBUFDATA10	28	
9	HBUFDATA4	29	
10	HBUFDATA11	30	GND
11	HBUFDATA3	31	HDD-IRQ
12	HBUFDATA12	32	NC
13	HBUFDATA2	33	DA1
14	HBUFDATA13	34	GND
15	HBUFDATA1	35	DA0
16	HBUFDATA14	36	DA2
17	HBUFDATA0	37	HDDCS-0
18	HBUFDATA15	38	HDDCS-1
19	GND	39	IDE-DASP
20	NC	40	GND

AV Connector – PL340			
Pin	Description	Pin	Description
1	+12V	11	C
2	GND	12	FBOUTENC
3	+5V	13	AV_INT
4	GND	14	GND
5	Red	15	LEFT AUDIO
6	Green	16	RIGHT AUDIO
7	Blue	17	GND
8	GND	18	GND
9	CVBS	19	SDA0
10	Y	20	SCL0

SCART CONNECTION



TV Scart Socket

TV Scart Socket –PL101			
Pin	Description	Pin	Description
1	Audio Right Output	12	No Connection
2	No Connection	13	GND
3	Audio Left Output	14	GND
4	GND	15	RED Output
5	GND	16	Fast Blanking Output
6	No Connection	17	GND
7	BLUE Output	18	GND
8	Function Switching Output	19	CVBS Output
9	GND	20	No Connection
10	No Connection	21	GND
11	GREEN Output		

VCR Scart Socket

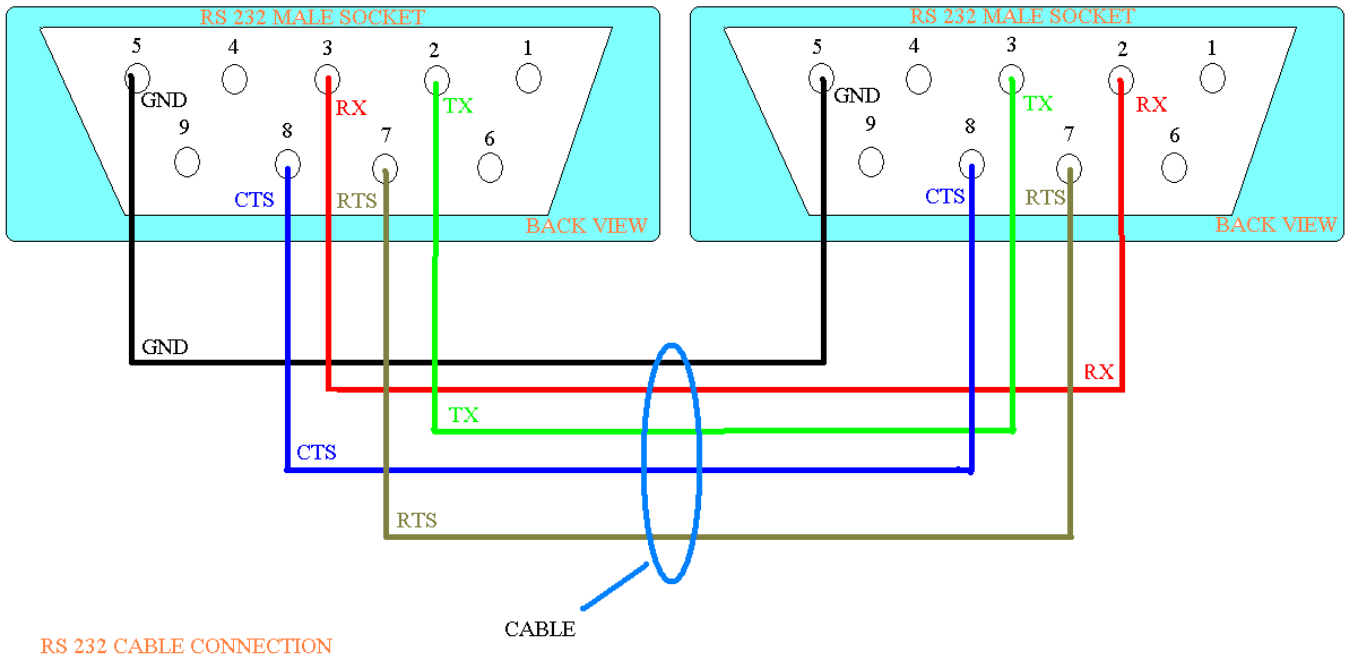
VCR Scart Socket - PL100			
Pin	Description	Pin	Description
1	Audio Right Output	12	No Connection
2	Audio Right Input	13	GND
3	Audio Left Output	14	GND
4	GND	15	No Connection
5	GND	16	No Connection
6	Audio Left Input	17	GND
7	No Connection	18	GND
8	Function Switching Input	19	CVBS Output
9	GND	20	CVBS Input
10	No Connection	21	GND
11	No Connection		

RS232 Serial Port

RS232 Header – JK_DSUB_9			
Pin	Description	Pin	Description
1	-	2	-
3	TXD	4	CTS
5	RXD	6	RTS
7	-	8	-
9	GND		

RCA (Audio and Composite Video) Connector

A/V Connector – JK1	
Pin	Description
1	RIGHT AUDIO
2	LEFT AUDIO
3	SPDIF AUDIO



RS 232 CABLE CONNECTION

Rs232 Test :

You connect the jumper to Rx output and Tx output. You press the “OK” key on the remote commander then you can see “tESt” at the front display. You release the “OK” key on the remote commander then you can see “Err” at the front display.

TECHNICAL SPECIFICATIONS

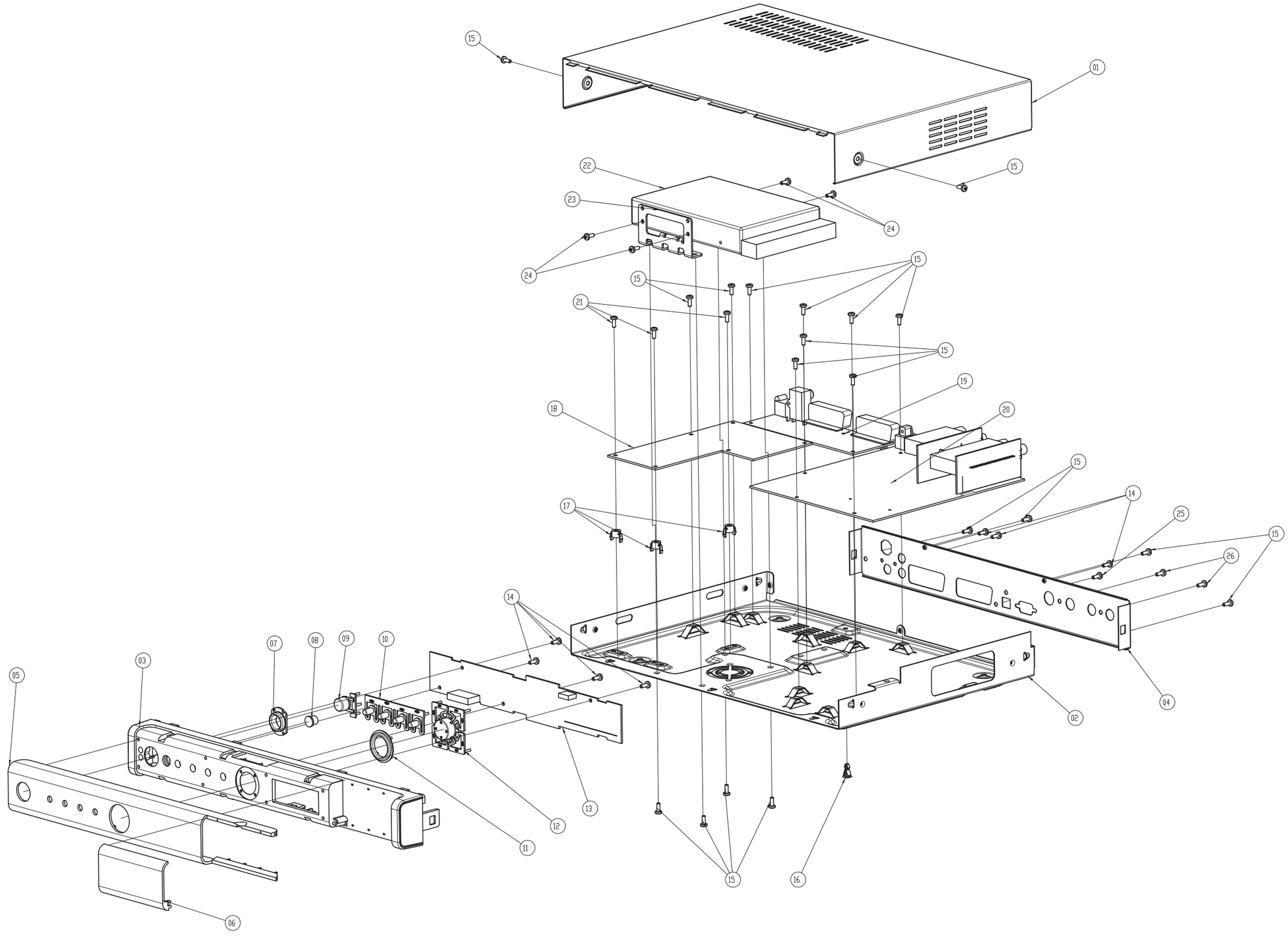
GENERAL CHARACTERISTICS	
Supply Voltage	220 - 240 V AC ~ 50Hz
Input Frequency	470Mhz-862Mhz
Maximum Power consumption	19W
Operating temperature	5ºC to +45ºC
Storage temperature	-15ºC to +55ºC
Humidity	25 to 75 % rel
Physical dimensions	360x280x48 mm
Weight	2820 g
HARDWARE CONFIGURATION	
Main Processor	STi5100
Flash Memory	4 MB
SDRAM	32 MB
DIGITAL CAPABILITIES	
Transmission Standards	DVB, MPEG2
DEMODULATION	
COFDM	with 2K/8K FFT mode.
FEC	for all DVB Modes.(Automatically found)
VIDEO	
ALL MPEG-2 MP@ML Video Decoder	
Aspect Ratio	4:3, 16:9 with pan vector
RGB analogue outputs.	BW ≥ 5MHz at 0.5 to 5 MHz sweep signal
CVBS analogue output.	
AUDIO	
MPEG1 Layer 1 and 2	
Sampling frequencies supported	32 kHz, 44.1 kHz, or 48 kHz.
Output can be programmed as STEREO, LEFT only or RIGHT only (on both outputs). This is useful for dual mono channels in order to select the correct sound track, which is stored for every channel.	
Wide dynamic range	16-bit resolution

REMOTE CONTROL	
Operating Distance	10m Max.
Batteries	2x1.5V Micro (R-03/AAA)
TUNERS	
2 xRF In :	IEC-type, female (75Ohm)
2 x RF Out (loop through) :	IEC-type, male (75Ohm)
FRONT PANEL	
Display	VFD
Remote Control Keys	Standby ON/OFF,Record,Play, Menu, OK,PR+ / PR-, V+ / V -,Standby Led, Record Led,
	1 Slot CI (Opt.), 1 Slot Smart Card (Opt.),USB2.0 connector (Opt.)
AUDIO R / L	
Connector	2 x RCA (R + L)
Output	0.5 Vrms 0dBfs / Z = 10kohm
DIGITAL AUDIO	
Output	Optik SPDIF
A / V & DATA IN / OUT	
Scart	TV scart, VCR scart
RGB Video Output	TV scart
RGB Video Intput	VCR scart
CVBS Video Output	TV scart, VCR scart
CVBS Video Input	VCR scart
Analog Audio Output	TV scart, RCA jack , VCR scart
Analog Audio Input	VCR scart
Digital Audio Output	Optic output
Data Interface	Scart RS 232, RS232 (max 115200 bps),9Pin

THE UPDATED PARTS LIST

FOR THIS MODEL IS

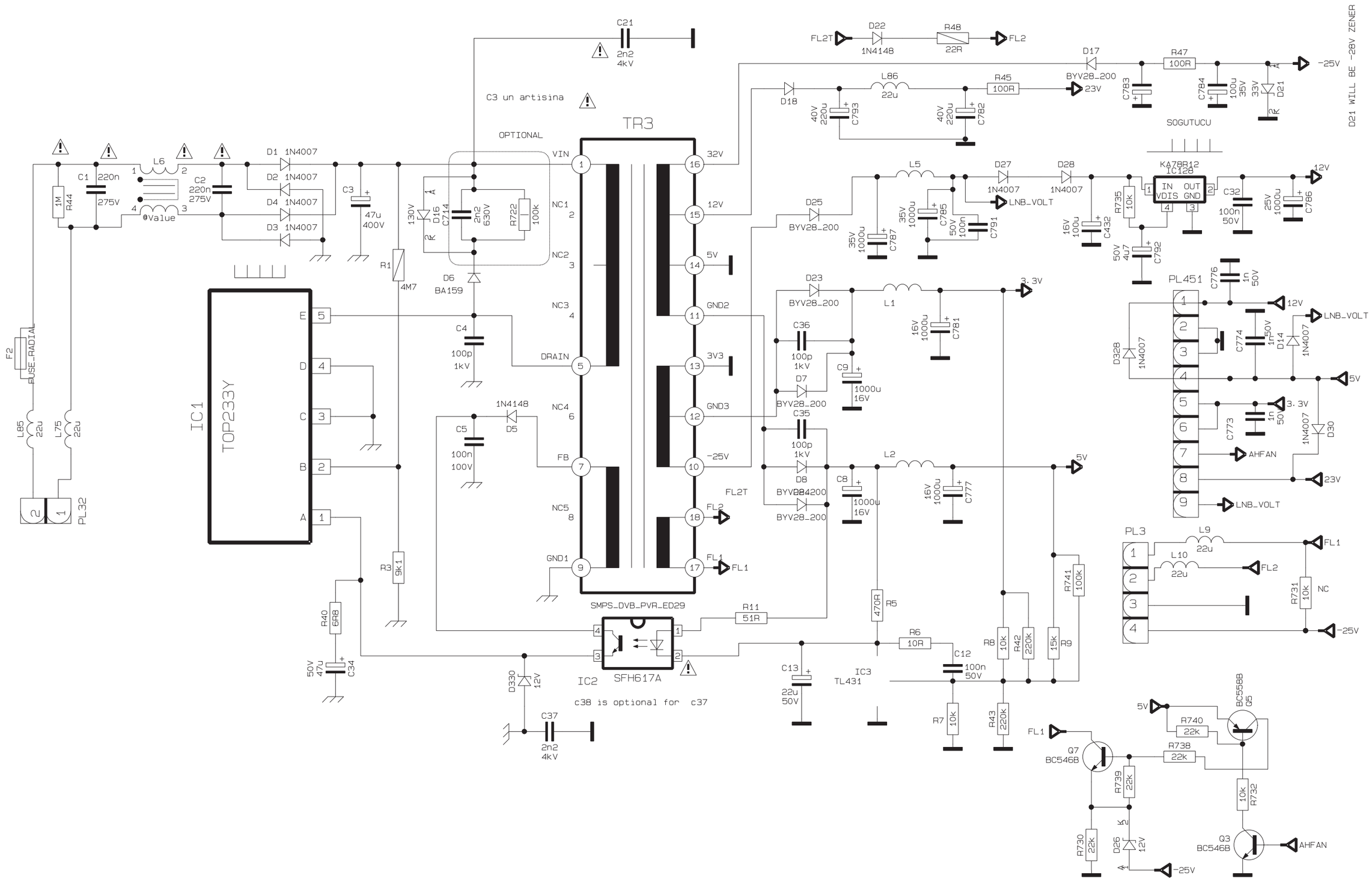
AVAILABLE ON ESTA



PVR1000

EXPLODED DIAGRAM

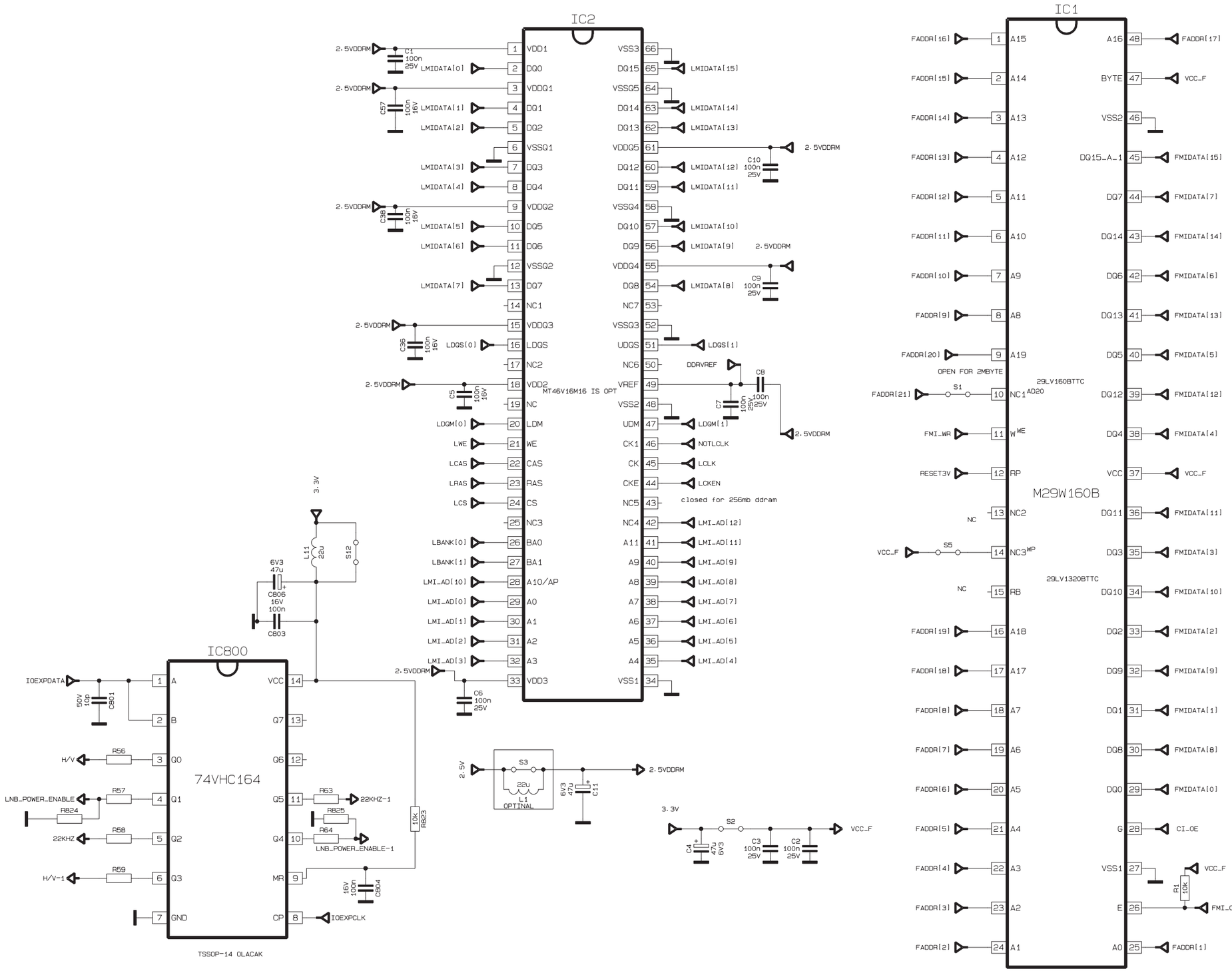
HITACHI



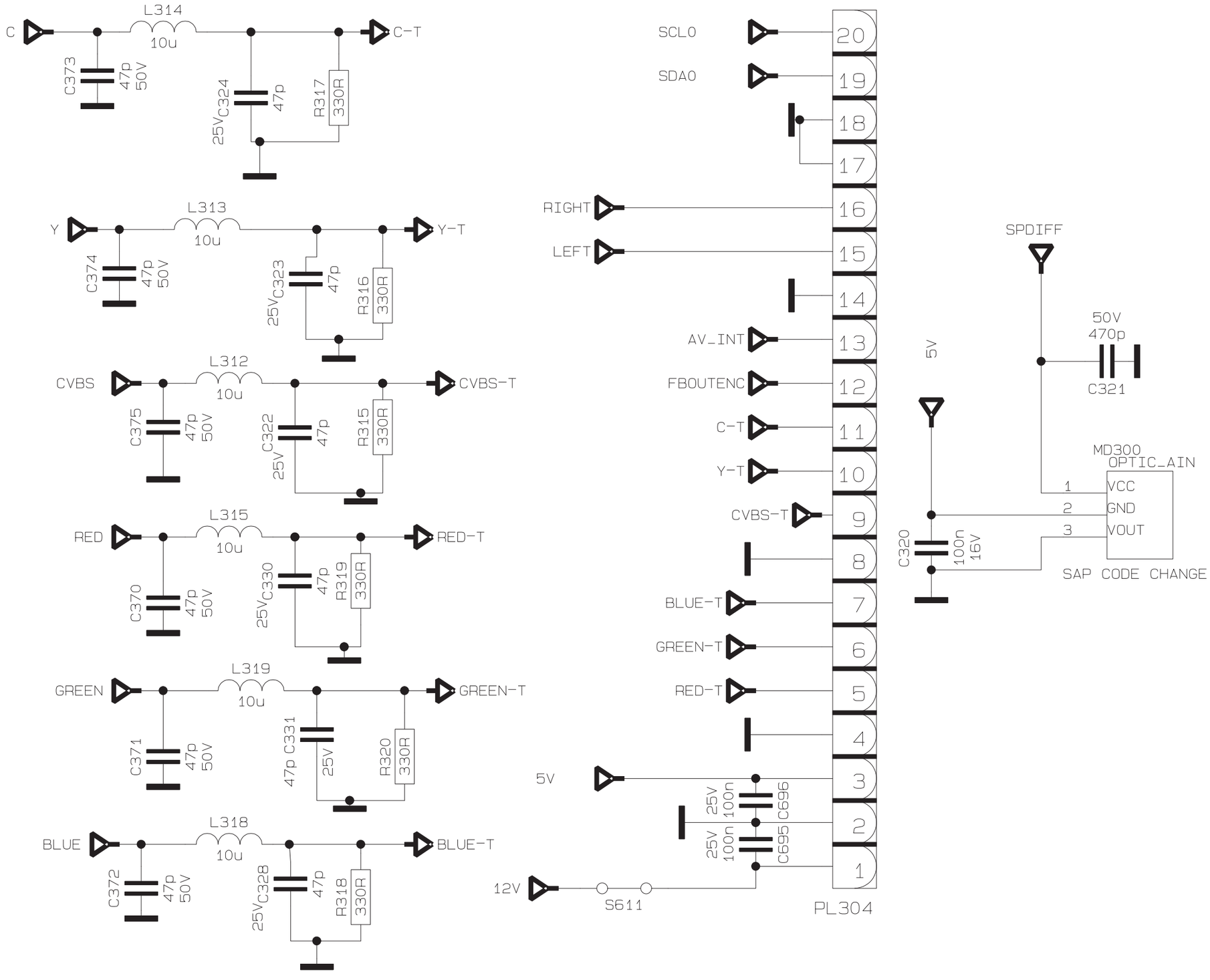
16PW36-2	POWER BOARD	HITACHI

IC101
STI5100

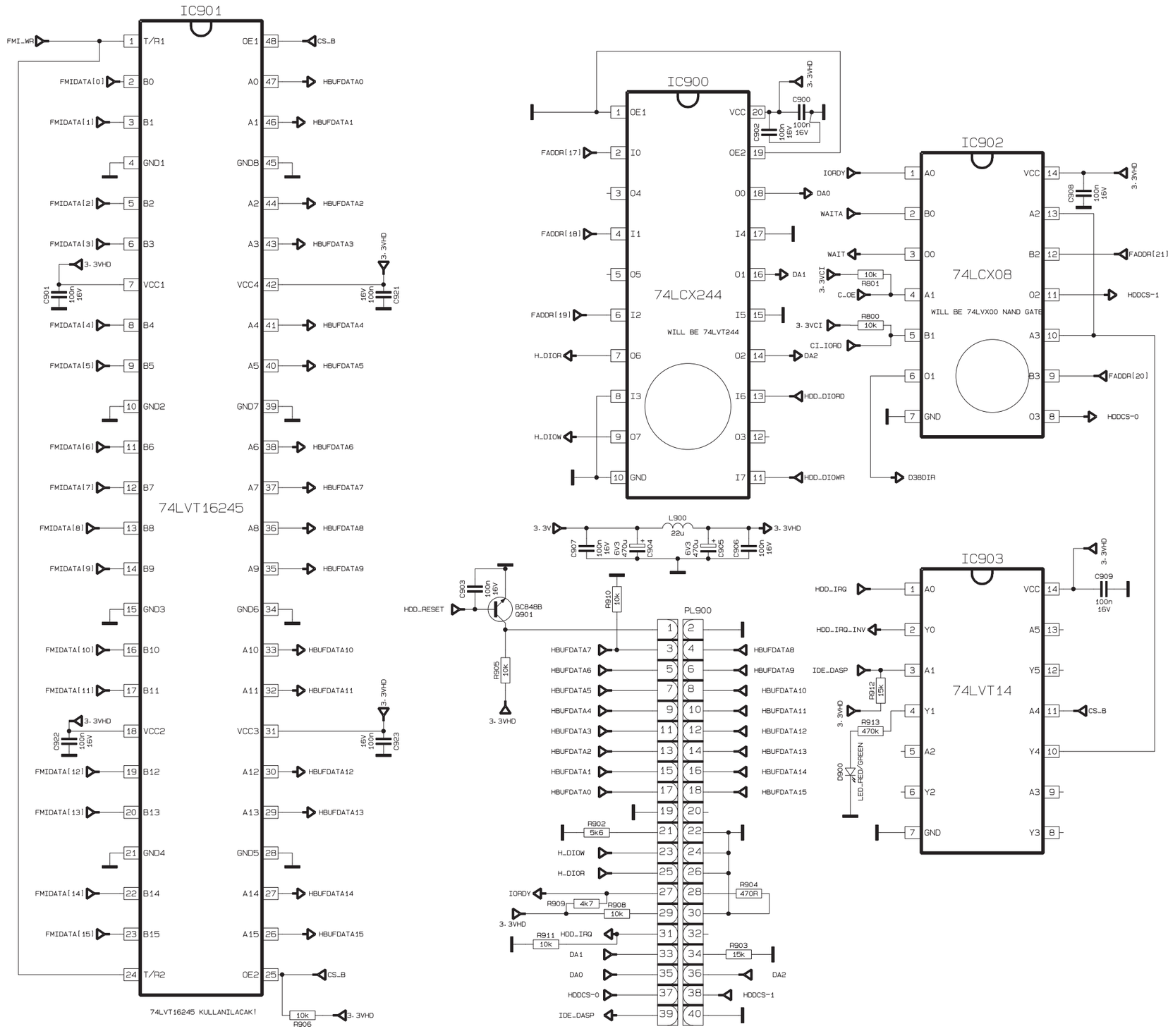
16MB31-1	MAIN BOARD - SHEET 1 of 8	HITACHI



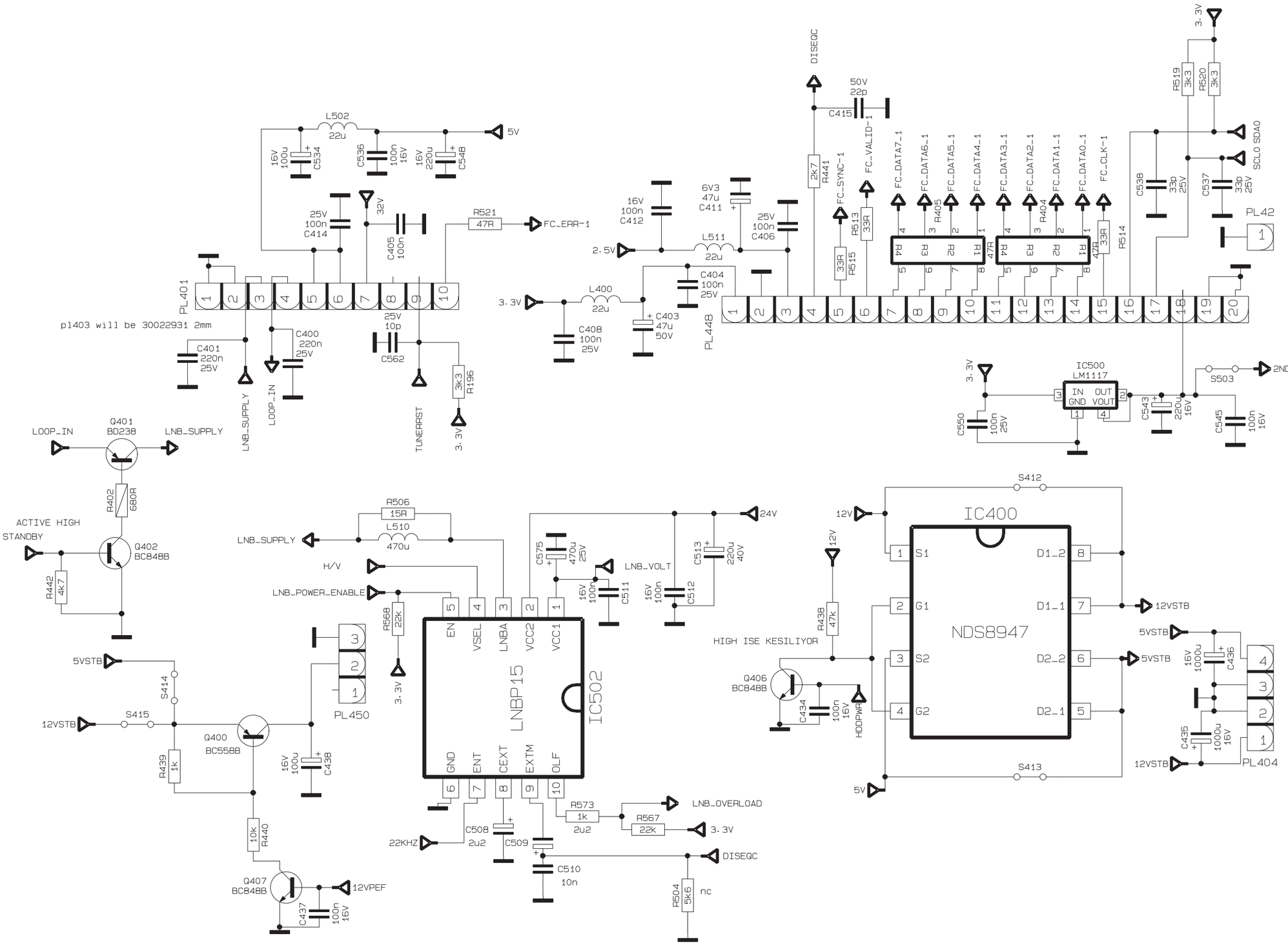
16MB31-1	MAIN BOARD - SHEET 2 of 8	HITACHI



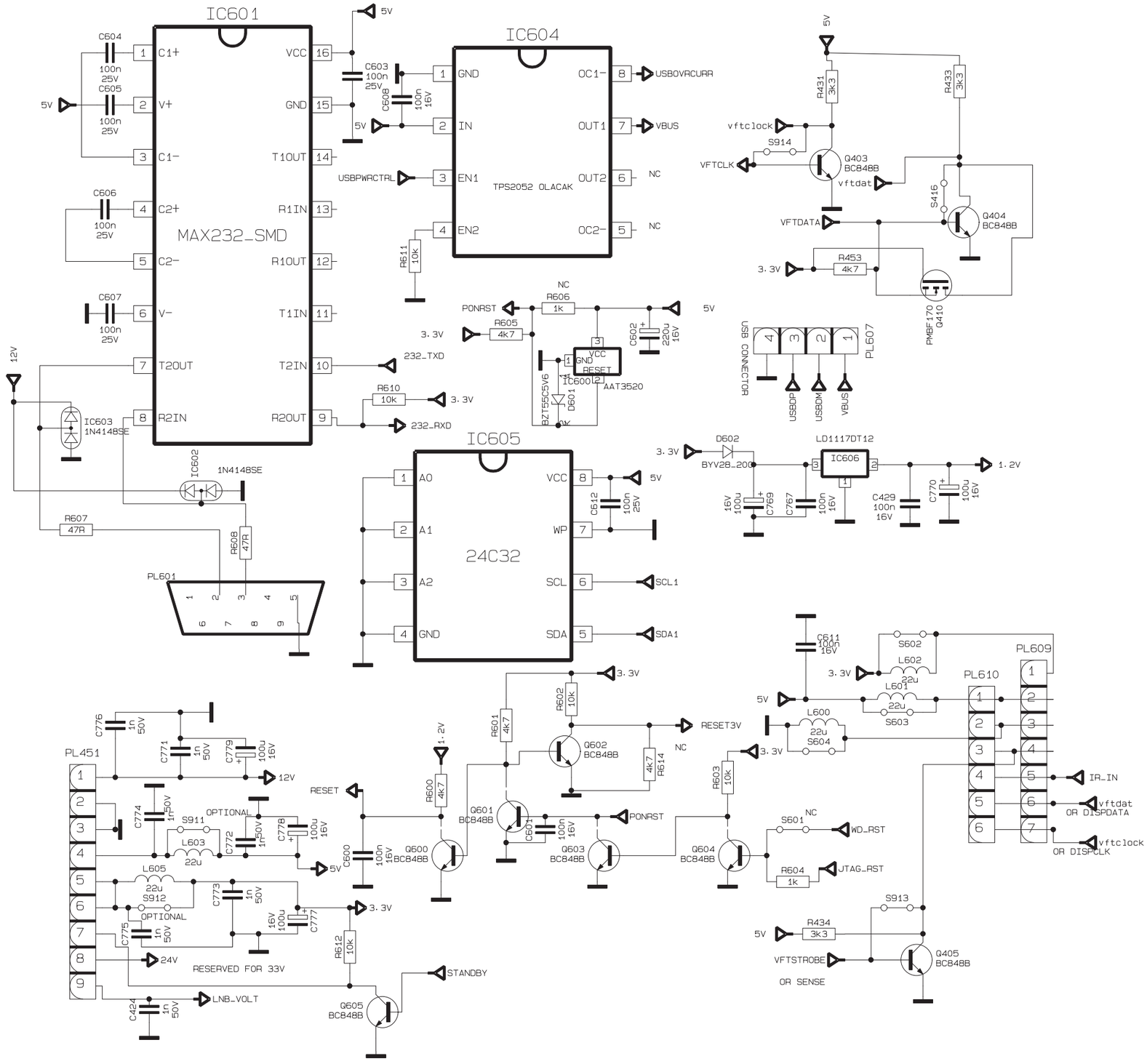
16MB31-1	MAIN BOARD - SHEET 3 of 8	HITACHI



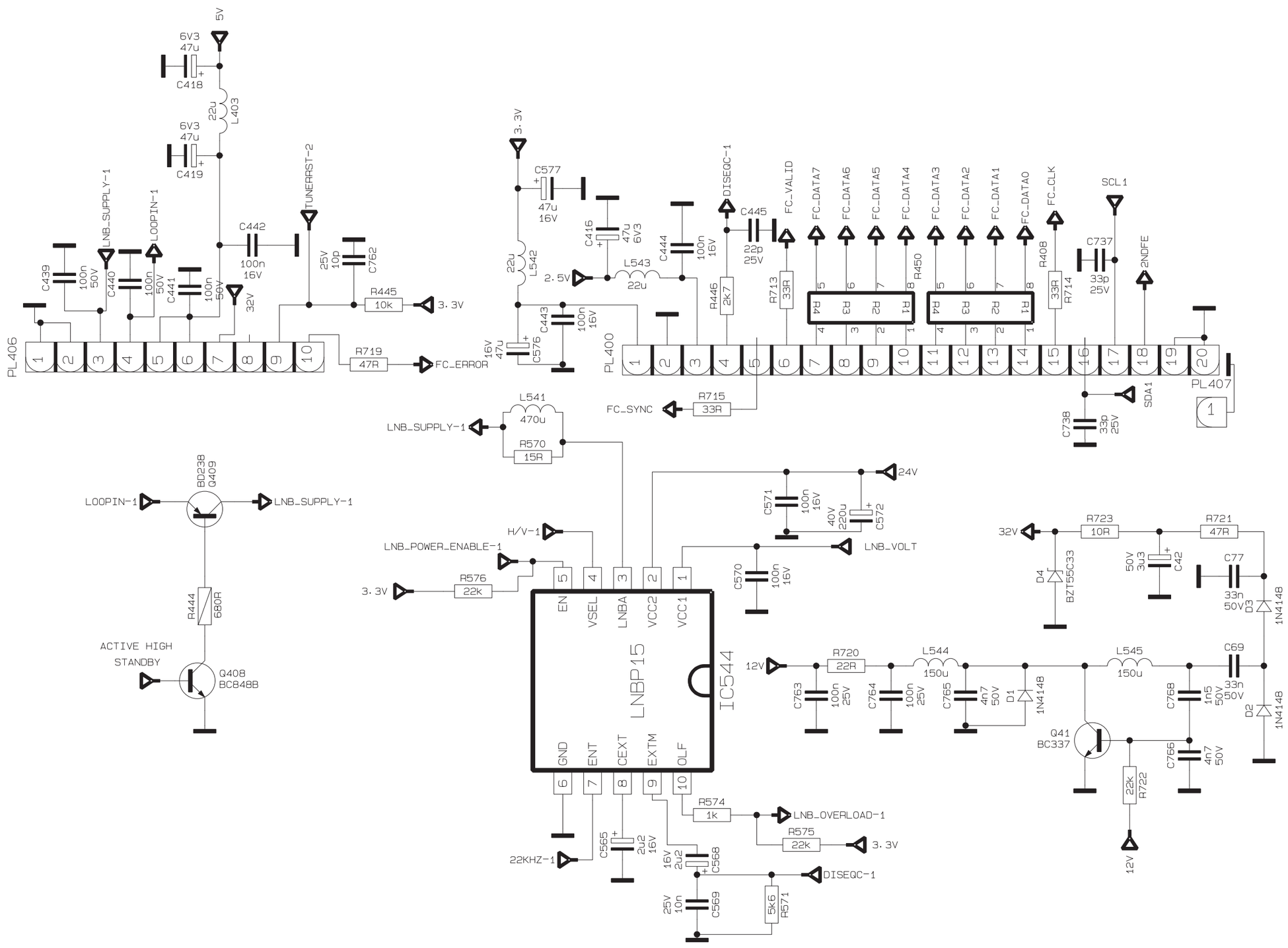
16MB31-1	MAIN BOARD - SHEET 4 of 8	HITACHI



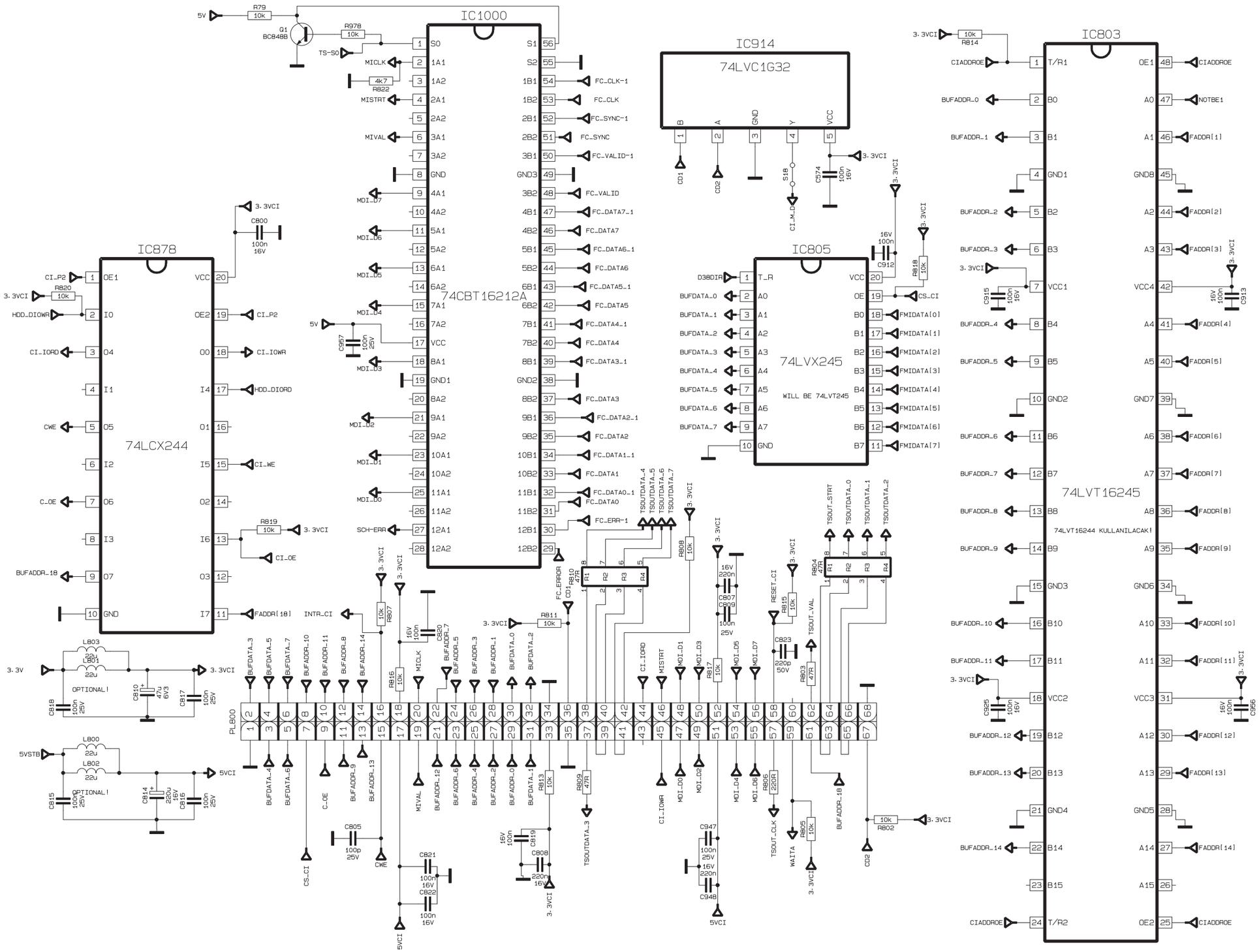
16MB31-1	MAIN BOARD - SHEET 5 of 8	HITACHI



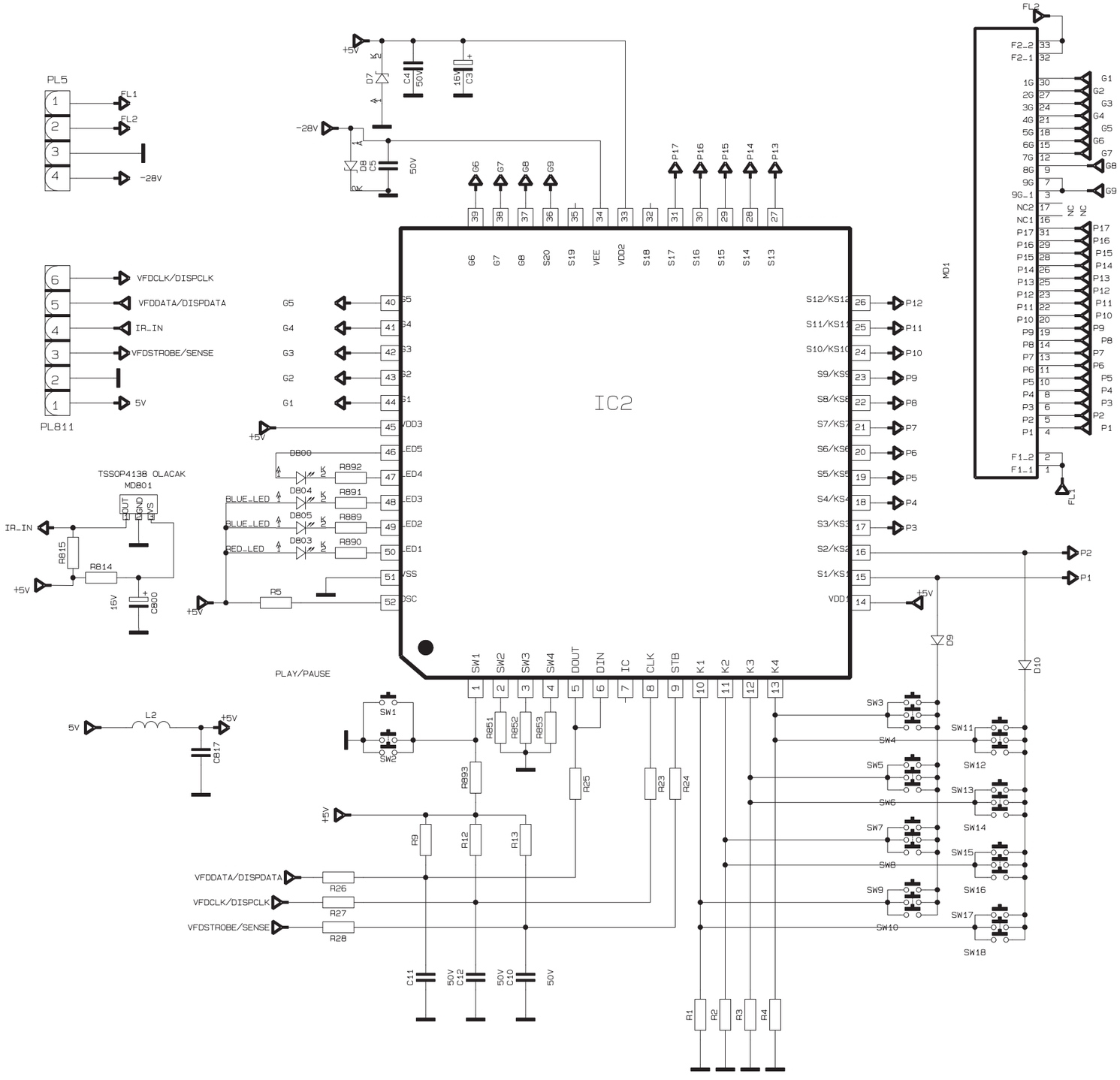
16MB31-1	MAIN BOARD - SHEET 6 of 8	HITACHI



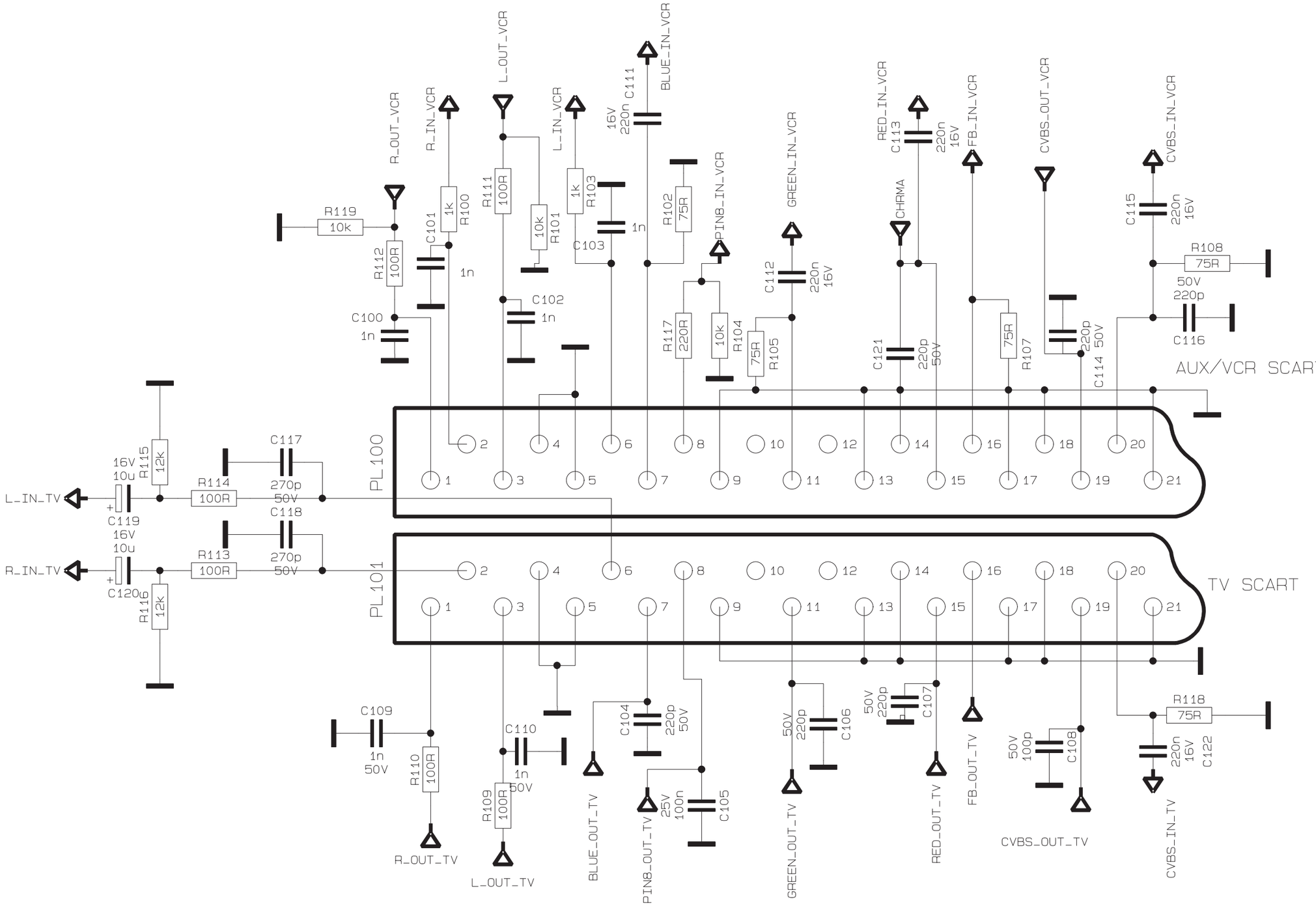
16MB31-1	MAIN BOARD - SHEET 7 of 8	HITACHI



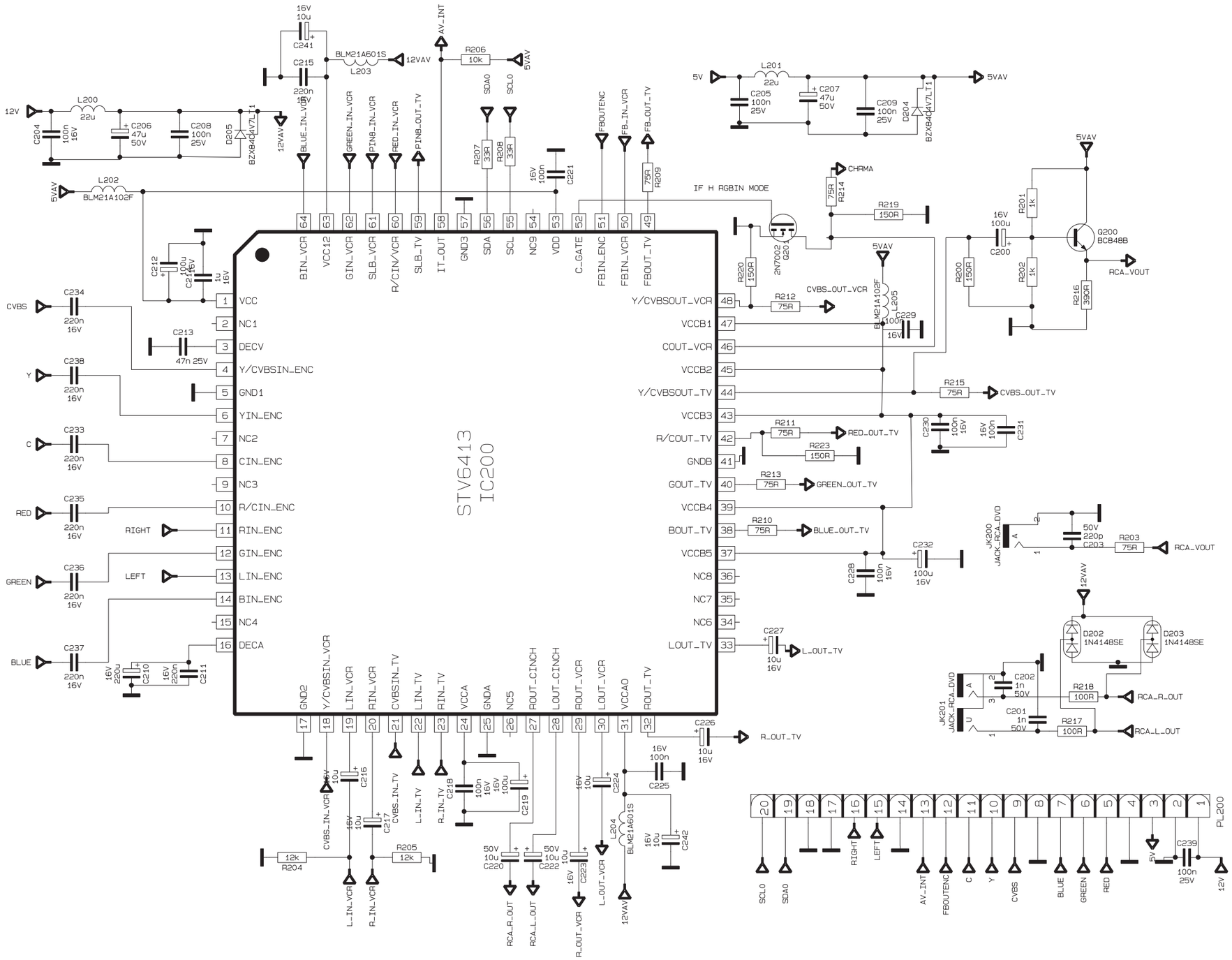
16MB31-1	MAIN BOARD - SHEET 8 of 8	HITACHI

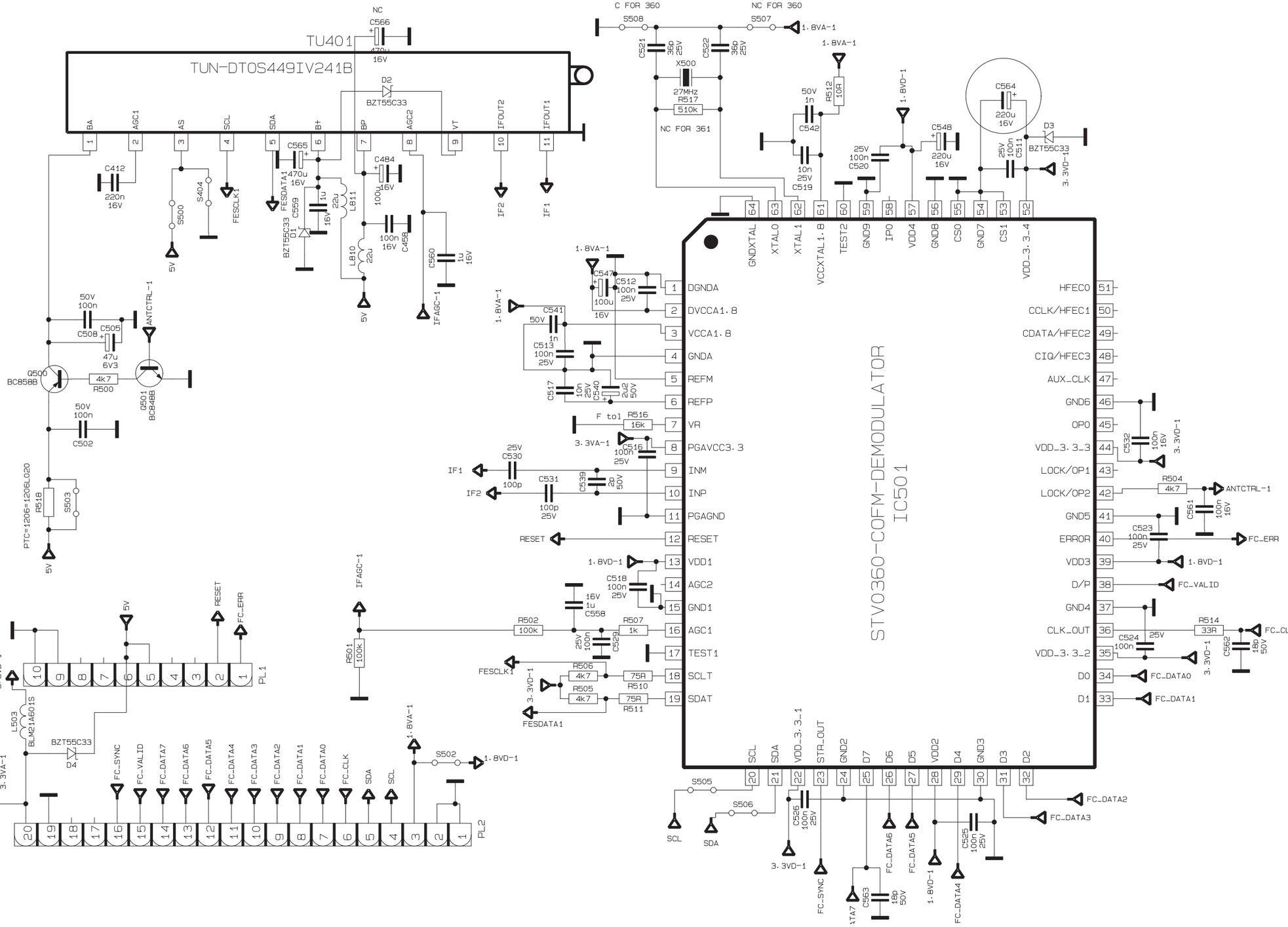


16FP38-3	FRONT BOARD	HITACHI



16SC31-2	AV BOARD - SHEET 1 of 2	HITACHI


STV6413
IC200
VCC
NC1
DECV
Y/CVBSIN_ENC
GND1
YIN_ENC
NC2
CIN_ENC
NC3
R/CIN_ENC
RIN_ENC
GIN_ENC
LIN_ENC
BIN_ENC
NC4
DECA
Y/CVBSOUT_VCR
VCCB1
COUT_VCR
VCCB2
Y/CVBSOUT_TV
VCCB3
R/COUT_TV
GNDB
GOUT_TV
VCCB4
BOUT_TV
VCCB5
NC8
NC7
NC6
LOUT_TV
BIN_VCR
VCC12
GIN_VCR
SLB_VCR
R/CIN/VCR
SLB_TV
IT_OUT
GND3
SDA
SCL
NC9
VDD
C_GATE
FBIN_ENC
FBIN_VCR
FBOUT_TV
GND2
Y/CVBSIN_VCR
LIN_VCR
RIN_VCR
CVBSIN_TV
LIN_TV
RIN_TV
VCCA
GNDA
NC5
ROUT_CINCH
LOUT_CINCH
ROUT_VCR
LOUT_VCR
VCCAO
ROUT_TV
IF H RGBIN MODE
CHRMA
CVBS_OUT_VCR
CVBS_OUT_TV
RED_OUT_TV
GREEN_OUT_TV
BLUE_OUT_TV
L_OUT_TV
R_OUT_TV
RCA_VOUT
RCA_R_OUT
RCA_L_OUT
CVBS
Y
C
RED
RIGHT
BLUE
GREEN
LEFT
5V
12V
5VAV
12VAV
PL200
JK200 JACK_RCA_DVD
JK201 JACK_RCA_DVD
2N7002 Q201
Q200 BC848B


TU401
TUN-DT0S449IV241B
NC
C566
470u
16V
D2
BZT55C33
BA
AGC1
AS
SCL
SDA
B+
BP
AGC2
VT
IFOUT2
IFOUT1
C412
220n
16V
S500
S404
FESCLK1
C565
470u
16V
FESDATA1
BZT55C33
D1
C559
1u
16V
L811
22u
C484
100u
16V
L810
22u
100n
16V
C458
C560
1u
16V
IF2
IF1
IFAGC-1
5V
C FOR 360
NC FOR 360
S508
S507
1.8VA-1
C521
36p
25V
C522
36p
25V
X500
27MHz
R517
510k
NC FOR 361
R512
10R
50V
1n
C542
10n
25V
C519
1.8VD-1
25V
100n
C520
C548
220u
16V
C564
220u
16V
25V
100n
C511
D3
BZT55C33
3.3VD-1
GNDXTAL
XTALO
XTAL1
VCCXTAL1.8
TEST2
GND9
IP0
VDD4
GND8
CS0
GND7
CS1
VDD_3.3_4
C547
100u
16V
C512
100n
25V
C541
50V
1n
C513
100n
25V
C517
10n
25V
C540
2u2
50V
F tol
R516
16k
3.3VA-1
C516
100n
25V
C530
25V
100p
C531
100p
25V
C539
2p
50V
RESET
1.8VD-1
C518
100n
25V
16V
1u
C558
R502
100k
R507
1k
25V
100n
C529
R506
4k7
75R
R510
R505
4k7
75R
R511
FESDATA1
R501
100k
IFAGC-1
1
DGNDA
2
DVCCA1.8
3
VCCA1.8
4
GNDA
5
REFM
6
REFP
7
VR
8
PGAVCC3.3
9
INM
10
INP
11
PGAGND
12
RESET
13
VDD1
14
AGC2
15
GND1
16
AGC1
17
TEST1
18
SCLT
19
SDAT
STV0360-COFDM-DEMODULATOR
IC501
HFEC0
51
CCLK/HFEC1
50
CDATA/HFEC2
49
CIQ/HFEC3
48
AUX_CLK
47
GND6
46
OP0
45
VDD_3.3_3
44
LOCK/OP1
43
LOCK/OP2
42
GND5
41
ERROR
40
VDD3
39
D/P
38
GND4
37
CLK_OUT
36
VDD_3.3_2
35
D0
34
D1
33
C532
100n
16V
3.3VD-1
R504
4k7
ANTCTRL-1
C561
100n
16V
C523
100n
25V
FC_ERR
1.8VD-1
FC_VALID
R514
33R
FC_CLK
C524
100n
25V
C562
18p
50V
FC_DATA0
FC_DATA1
SCL
SDA
VDD_3.3_1
STR_OUT
GND2
D7
D6
D5
VDD2
D4
GND3
D3
D2
S505
S506
C526
100n
25V
C525
100n
25V
FC_DATA2
FC_DATA3
FC_DATA6
FC_DATA5
FC_DATA4
FC_SYNC
C563
18p
50V
1.8VD-1
3.3VD-1
50V
100n
C508
C505
47u
6V3
ANTCTRL-1
Q500
BC858B
4k7
R500
Q501
BC848B
C502
PTC=1206=1206L020
R518
S503
5V
L503
BLM21AG01S
BZT55C33
D4
3.3VA-1
PL1
PL2
FC_SYNC
FC_VALID
FC_DATA7
FC_DATA6
FC_DATA5
FC_DATA4
FC_DATA3
FC_DATA2
FC_DATA1
FC_DATA0
FC_CLK
SDA
SCL
S502
1.8VD-1

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